## WHAT IS CLAIMED IS:

1	1. A method for manufacturing composite substrates for semiconductor
2	devices, the method comprising:
3	providing a metal substrate, the metal substrate having a first diameter and
4	having a bonding surface;
. 5	bonding a plurality of tiles overlying the bonding surface, each of the tiles
6	being coupled to a portion of the bonding surface, each of the tiles having a shape and size to
7	be able to form an array configuration;
8	elevating a temperature of the plurality of tiles and metal substrate;
9	forming a eutectic bond between each of plurality of tiles and portion of the
10	bonding surface, whereupon the elevating of the temperature is provided while each of the
11	tiles is substantially stationary relative to the metal substrate;
12	forming a plurality of active devices on each of the plurality of tiles;
13	forming a plurality of openings through each of tiles, each of the openings
14	traversing through a portion of one of the tiles through a portion of the eutectic bond to a
15	portion of the metal substrate to form a via structure;
16	forming an interconnect layer to connect the portion of the one of the active
17	devices through the portion of the tile through the eutectic bond to the portion of the metal
18	substrate;
19	whereupon the interconnect layer that connects the portion of one of the active
20	devices through the portion of one of the tiles through the portion of the eutectic bond to the
21	portion of the metal substrate.
1	2. The method of claim 1 wherein the forming of the plurality of
2	openings in each of the tiles further comprises coating the plurality of active devices using a
3	photolithographic material and patterning the coating to form regions corresponding to the
4	openings.
•	of things.
. 1	3. The method of claim 2 wherein the patterning comprises an etching
2	process.
1	4. The method of claim 1 wherein each of the tiles comprises an entity
2	selected from gallium arsenide, indium phosphide, gallium nitride, and silicon carbide.
2	
. 1	5. The method of claim 1 wherein each of the openings is a via structure.

1	6. The method of claim 1 wherein the eutectic bond is provided using an
2	alloy selected from a low melting temperature metal including indium, tin and an oxidation-
3	resistant metal.
1	7. The method of claim 1 wherein the array configuration is an N by M
2	array of the tiles, each of the tiles being coupled to another tile.
1	8. The method of claim 1 wherein each of the openings is characterized
2	by an aspect ratio of greater than 2 to 1.
1	9. The method of claim 1 wherein the interconnect layer comprises gold
2	over platinum over titanium.
1	10. The method of claim 1 wherein the interconnect layer comprises a
2	barrier metal layer underlying a conductive layer.
1	11. The method of claim 1 wherein the metal substrate provides a ground
2	plane.
. 1	12. A method of manufacturing bonded substrates, the method comprising:
2	providing a metallic substrate, the metal substrate having a predetermined
3	thickness;
4	bonding a first thickness of compound semiconductor material overlying the
5	metallic substrate;
6	reducing a thickness of the first thickness of compound semiconductor
7	material to a second thickness; and
8	forming one or more via structures through a portion of the second thickness
9	of compound semiconductor material to a portion of the underlying metal substrate,
10	whereupon the via structure electrically connects to the metal substrate.
1	13. The method of claim 12 wherein the second thickness of compound
, 2	semiconductor substrate is less than 100 microns.
1	14. The method of claim 13 wherein the second thickness of compound
2	semiconductor material is unstable without the metal substrate.

1	15. The method of claim 13 wherein the via structure has an aspect ratio i
2	greater than 2 to 1.
1	16. The method of claim 12 wherein the metal substrate is characterized by
2	a first thermal expansion coefficient and the compound semiconductor is characterized by a
3	second thermal expansion coefficient, whereupon the first thermal expansion coefficient is
4	within a predetermined amount of the second thermal expansion coefficient.
1	17. The method of claim 12 wherein the predetermined amount is
2	characterized to prevent any damage to the compound semiconductor through a temperature
3	range from about room temperature to 550 Degrees Celsius.
1	18. The method of claim 12 further comprising processing the second
2	thickness of compound semiconductor through one or more manufacturing processes for
3	integrated circuits.
1	19. The method of claim 18 wherein the one or more manufacturing
2	processes includes at least an alloying process to form a contact between the compound
3	semiconductor and a metal layer.
1	20. The method of claim 19 wherein alloying process is an annealing
2	process.
1 ·	21. A method of manufacturing bonded substrates, the method comprising
2	providing a metallic substrate, the metallic substrate having a predetermined
3	thickness;
4	bonding a first thickness of compound semiconductor material overlying the
5	metallic substrate;
6	reducing a thickness of the first thickness of compound semiconductor
7	material to a second thickness; and
8	forming one or more trench structures through a portion of the second
9	thickness of the compound semiconductor through a side opposite of a backside of the
0	metallic substrate;
1	forming one or more metal structures within the one or more trench structure
2	to form and or more requestive via structures within the nortion of the second thickness of

14	the via structure electrically connects to the metal substrate.
1	22. A method of manufacturing bonded substrates, the method comprising:
2	providing a metallic substrate, the metal substrate having a predetermined
3	thickness;
4	bonding a first thickness of compound semiconductor material overlying the
5	metallic substrate;
6	reducing a thickness of the first thickness of compound semiconductor
7	material to a second thickness; and
8.	forming a trench region surrounding a portion of the second thickness of the
9	compound semiconductor material; and
10	forming a conductive material within the trench region to isolate the portion of
11	the second thickness of the compound semiconductor using the conductive material in the
12	trench region and a portion of the underlying metallic substrate.
1	23. The method of claim 22 exposing an upper portion of the portion of the
2	second thickness of the compound semiconductor.
1	24. The method of claim 22 further comprising forming an insulating layer
2	overlying the exposed upper portion.
1	25. The method of claim 24 further comprising forming a metal layer
2	overlying the insulating layer and connecting to the conductive material in the trench region
3	to enclose the portion of the second thickness of the compound semiconductor.
1	26. A substrate structure for high frequency devices, the structure
2	comprising:
3	a metallic substrate, the metallic substrate being a ground plane for a high
4	frequency amplifying device operable at a frequency greater than 10 G Hz;
5	a compound semiconductor material bonded to the metallic substrate;
6	one or more via structures for ground connections formed within portions of
7	the compound semiconductor material, the one or more via structures being electrically
8	connected to the metallic substrate:

compound semiconductor material to a portion of the underlying metal substrate, whereupon

9	whereupon the one or more via structures are configured to provide a desired
0	reactance to provide a universal ground reference, the universal ground reference is within a
1	predetermined amount.
1	27. The structure of claim 26 wherein predetermined amount is less than
2	one quarter of the wavelength of the operating frequency of the circuit.
1	28. The structure of claim 26 wherein the desired reactance ranges from
2	about 0.01 ohm to about 1 ohm.
1	29. An integrated circuit device structure, the integrated circuit device
2	structure comprising:
3	a metallic substrate, the metal substrate having a predetermined thickness and
4	a predetermined thermal conductivity;
5	a thickness of compound semiconductor material bonded to a surface
6	overlying the metallic substrate; and
<b>7</b>	a trench region disposed within a portion of the thickness of the compound
8	semiconductor material and extending to a portion of the metallic substrate; and
9	a thermal conductive material formed within the trench region and thermally
0	coupled to the portion of the metallic substrate, the thermal conductive material being
1	coupled to the portion of the thickness of the compound semiconductor to redistribute
2	thermal energy among the portion of the compound semiconductor, the thermal conductive
3	material, and the metallic substrate.
1	30. The structure of claim 29 wherein the trench region surrounds the
2	portion of the thickness of the compound semiconductor material.
1	The structure of claim 29 wherein the substrate is a heat sink.
1	32. The structure of claim 29 wherein the redistributed thermal energy

provides the portion of the compound semiconductor free from one or more hot spots.